UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/634,045	08/08/2000	Drew Eric Wingard	02998.P011	5608

7590 07/17/2006

Maria McCormack Sobrino
Blakely Sokoloff Taylor & Zafman LLP
12400 Wilshire Boulevard
7th Floor
Los Angeles, CA 90025

EXAMINER	
THOMPSON, ANNETTE M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/634,045	WINGARD ET AL.	
	Examiner	Art Unit	
	A. M. Thompson	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 August 2000 and 26 September 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/16/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the Applicants' Supplemental Appeal Brief and Reply Brief filed on 10/06/2005, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

Supervisory Patent Examiner (SPE) Jack Chiang has approved of reopening prosecution. Accordingly, this concurring signature is indicated, infra.

2. This application has been examined. Claims 12-22 are pending.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Rejection of claims 12-22 applying Guccione et al.

4. **Claims 12-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guccione et al. (Guccione), U.S. Patent 6,216,259.** Guccione teaches a system and method for run-time reconfiguration of a programmable logic device using routing cores. Guccione does not explicitly disclose a run-time reconfiguration wherein interface signal carries are selectively physically present or not. However, Guccione does disclose generating router core definitions that generate and define, at run-time, router core definitions that define couplings between logic cores (Guccione, col. 2, ll. 30-45) It would been obvious to one of ordinary skill in the art at the time of Applicants' invention that a selectively present physical interface connection is tantamount or al least functionally similar to the router core determination and definition of interface connections at run-time.

5. Pursuant to claim 12 which recites [a] computer core having an interface to communicate with other cores wherein the interface contains a plurality of interface signal carriers that are configurable (col. 2, ll. 30-35 wherein compilation is suggested by "run-time reconfiguration"), at compilation, (see also col. 2, ll. 40-45, wherein the routing core generators generate at least one router core definition that defines a coupling of logic cores) (see also Fig. 3, #306) such that at least one of the interface signal carriers is selectively physically present in the interface or not physically present (col. 5, ll. 49-54, wherein the routing cores provide necessary information to connect logic cores), wherein not physically present means that a route connection is not generated for an interface signal carrier selected to be not physically present (col. 7, ll. 5-15 discloses the configuration of router connections, the generation of which has

variable connections depending on the router core definitions; see also col. 15, ll. 1-4 wherein the router core definition defines a coupling of the logic cores in the programmable logic device).

6. Pursuant to claim 13 wherein the computer core is a core on a system on a chip and the other cores also belong to that system on a chip (col. 2, ll. 35-48, wherein the logic cores are part of an FPGA).

7. Pursuant to claim 14, wherein a first interface signal carrier is further configured to support different levels of functionality for the interface (col. 15, claim 9 which details the various levels of interface configurations that may be defined).

8. Pursuant to claim 15, wherein a signal carrier width of the first interface signal carrier is also configurable to support different signal widths (col. 7, ll. 10-15 disclose that signal lines are programmable which would suggest that variable width configurations are within the scope).

9. Pursuant to claim 16, which recites a core on a system on a chip (col. 2, ll. 30-40) having an interface, wherein the interface contains a plurality of interface signal carriers that are configurable, at compilation, (col. 5, ll. 25-35 discloses run-time reconfiguration) such that at least one of a first interface signal carrier is configurable to support different levels of functionality for the interface (col. 7, ll. 10-15 disclose that signal lines are programmable which suggest the existence of variable width configurations).

10. Pursuant to claim 17, wherein a signal carrier width of the first interface signal carrier is also configurable to support different signal widths (col. 7, ll. 10-15 disclose

that signal lines are programmable which would suggest that variable width configurations are within the scope).

11. Pursuant to claim 18, wherein a first interface signal carrier is configurable, at compilation, such that the first interface signal carrier is selectively physically present in the interface or not physically present (col. 5, ll. 49-56)

12. Pursuant to claim 19, which recites [a] method for generating at compilation a core interface (col. 5, ll. 40-48) for a system on a chip to enable re-use of the core with a different interface configuration (col. 5, ll. 49-57), the method comprising: providing configurable source code representative of the core interface for the system on a chip (col. 2, ll. 40-43, wherein the logic core generators generate define the logic cores; see also col. 4, ll. 39-62) and identifying parameters of the core interface (col. 12, ll. 39-47); defining configuration parameters of the core interface (col. 12, ll. 34-36); generating the core interface for the system on a chip (col. 12, ll. 34-38 discloses the core) from the configurable source code representative of the core interface and the identified parameters of the core interface configurable in accordance with the defined configuration parameters of the core interface (col. 13 – col. 14, line 44 represents the configurable source code).

13. Pursuant to claim 20, wherein at least one of the configuration parameters of the core interface is defining whether a first signal carrier will be physically present in the core interface or not physically present (col. 2, ll. 35-37; col. 5, ll. 48-52, wherein the router cores establish connections for selected ones of the logic cores).

14. Pursuant to claim 21, wherein at least one of the configuration parameters of the core interface is defining different levels of functionality that the core interface supports through a plurality of signal interface carriers (col. 5, ll. 49-57).

15. Pursuant to claim 22, wherein at least one of the configuration parameters of the core interface is defining a signal width of a first interface signal carrier (col. 7, ll. 10-15 disclose that signal lines are programmable which suggest the existence of variable width configurations).

Rejection of claims 12-22 applying Blodget

16. **Claims 12-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blodget, U.S. Patent 6,510,546.** Blodget discloses a method and apparatus for developing parameterizable logic cores at compilation (Abstract, col. 4, ll. 3-17). In Blodget, program code representative of a logic core function (col. 4, ll. 3-18) may be changed or parameterized at compilation (run-time) to define a variable interface (interconnect) width or size. Blodget also discloses an interface that supports different levels of functionality (col. 4, ll. 3-18). Blodget, however, does not explicitly disclose or use Applicants' terminology of "first signal interface carrier" or "interface signal carrier being physically present". However, Blodget discloses interconnect resources and the editing of program code to define specific interconnect resources (i.e. define what is physically present or not) at run-time (col. 5, ll. 35-40), and it would have been obvious to one of ordinary skill in the art at the time of Applicants' invention that Blodget's disclosure of defining interface elements at run-time suggests and is at least tantamount to determining whether or not a route connection should be generated for an interface.

17. Pursuant to claim 12 which recites [a] computer core having an interface to communicate with other cores wherein the interface contains a plurality of interface signal carriers that are configurable (col. 2, ll. 41-53 wherein at compilation is suggested by "run-time reconfiguration"), at compilation, such that at least one of the interface signal carriers is selectively physically present in the interface or not physically present (col. 5, ll. 15-17, wherein a bit interface program is called to program specific interconnect resources), wherein not physically present means that a route connection is not generated for an interface signal carrier selected to be not physically present (see also, col. 5, ll. 34-48, wherein the interconnect resources are programmed in the code; see also col. 10, ll. 8-13 wherein output pins and input pins are defined).

18. Pursuant to claim 13 wherein the computer core is a core on a system on a chip and the other cores also belong to that system on a chip (col. 3, line 64 to col. 4, line 2).

19. Pursuant to claim 14, wherein a first interface signal carrier is further configured to support different levels of functionality for the interface (col. 4, ll. 6-18 (". . .some of the functions in the set may be programmed for certain devices. ..").

20. Pursuant to claim 15, wherein a signal carrier width of the first interface signal carrier is also configurable to support different signal widths (col. 5, ll. 43-50, wherein the interconnect resource can be changed via an index).

21. Pursuant to claim 16, which recites a core on a system on a chip having an interface, wherein the interface contains a plurality of interface signal carriers that are configurable, at compilation, such that at least one of a first interface signal carrier is configurable to support different levels of functionality for the interface (col. 4, ll. 3-15).

22. Pursuant to claim 17, wherein a signal carrier width of the first interface signal carrier is also configurable to support different signal widths (col. 5, ll. 43-50).

23. Pursuant to claim 18, wherein a first interface signal carrier is configurable, at compilation, such that the first interface signal carrier is selectively physically present in the interface or not physically present.

24. Pursuant to claim 19, which recites [a] method for generating at compilation a core interface for a system on a chip to enable re-use of the core with a different interface configuration (col. 4, ll. 65-67), the method comprising: providing configurable source code representative of the core interface for the system on a chip and identifying parameters of the core interface; defining configuration parameters of the core interface; generating the core interface for the system on a chip from the configurable source code representative of the core interface and the identified parameters of the core interface configurable in accordance with the defined configuration parameters of the core interface (col. 5, line 60 to col. 6, line 63).

25. Pursuant to claim 20, wherein at least one of the configuration parameters of the core interface is defining whether a first signal carrier will be physically present in the core interface or not physically present (col. 5, ll. 34-50).

26. Pursuant to claim 21, wherein at least one of the configuration parameters of the core interface is defining different levels of functionality that the core interface supports through a plurality of signal interface carriers (col. 4, ll. 3-18).

27. Pursuant to claim 22, wherein at least one of the configuration parameters of the core interface is defining a signal width of a first interface signal carrier (col. 5, ll. 34-50).

Remarks

28. Applicants additional new information in the Supplemental Appeal Brief of October 6, 2005 at page 5, first full paragraph, alleges that the claims are different from the prior art and that neither the prior art of Guccione (U.S.P. 6,216,259) or Blodget (U.S.P. 6,510,546) teaches or suggests Applicants' invention. The prosecution history of this application suggests otherwise: After transfer of this application to Art Unit 2825, Guccione '259 was used in a 35 USC 102(e) rejection of pending claims 1-11. In response to the rejection, Applicants amended by canceling claims 1-11 and adding new claims 12-22. Examiner then chose to use the prior art of Blodget '456 to reject new claims 12-22. Applicants did not traverse, but rather submitted a declaration under 37 CFR 1.131 to antedate the Blodget '456 reference. Examiner has determined that Applicants' declaration is insufficiently substantive and Applicants have appealed that determination. However, even if the Blodget '456 reference was disqualified as prior art, the Guccione '259 reference would still read on Applicants' claims 12-22. Therefore, in the interest of compact prosecution, prosecution has been reopened now to add one more ground of rejection utilizing Guccione '259 rather than waiting until a decision on appeal is rendered.

Conclusion

29. Any inquiry concerning this communication or earlier communications should be directed to Examiner A.M. Thompson whose telephone number is (571) 272-1909. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 4:30 p.m..

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

30. Responses to this action should be mailed to the appropriate mail stop:

Mail Stop _____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to:

(571) 273-8300, (for all **OFFICIAL** communications intended for entry)

A. M. THOMPSON
Primary Examiner
Technology Center 2800

JACK CHIANG
SUPERVISORY PATENT EXAMINER